UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,146	05/11/2001	Jun Li	SPLX.P0050	6790

23349 7590 01/24/2003

STATTLER JOHANSEN & ADELI
P O BOX 51860
PALO ALTO, CA 94303

EXAMINER
SIEK, VUTHE

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,146	LI ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- Th MAILING DATE of this communication app ars on th cover sheet with th correspond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25* is/are allowed.

6)☒ Claim(s) *1,5,8,10,13,17 and 22* is/are rejected.

7)☒ Claim(s) *2-4,6,7,9,11,12,14-16,18-21,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 09/854,146 filed on 05/11/2001. Claims 1-24 remain pending in the application.

Specification

2. The disclosure is objected to because of the following informalities: page, line "switch from 1 to or 0 to 1" should be –switch from 1 to 0 or 0 to 1–.

Appropriate correction is required.

Claim Objections

3. Claims 10, 22 and 24 are objected to because of the following informalities: as to claims 10 and 22, phrases "determining **operation** of said circuit" and "...based on **operation**..." are not clear to as what operation is specifically referred to. Claim 24 should be dependent on claim 23. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5, 8, 10, 13, 17 and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Muddu (6,314,546).

6. As to claims 1, 8 and 13, Muddu teaches estimating interconnect capacitive effects including determining an effective capacitance that represents the interconnect capacitive effects at an output of a driving gate, where the effective capacitance

estimation precedes by a gate load modeling. Estimating the interconnect capacitive effects includes modeling the gate using an equivalent circuit, and modeling the gate load at an output of the gate includes determining RC model parameters that represent the load at the output of the gate output. These parameters are associated with response at the gate output. Muddu teaches determining delay taking accounts for the input voltage waveform (input signal slew rate), voltage response at the gate output and RC model parameters. The effective capacitance estimation method further includes modeling a single capacitance load at the output of the gate, where the single capacitive load modeling includes determining a gate delay for a threshold time at a threshold voltage. The effective capacitance is then derived taking into account the single capacitance, a total capacitance of the gate load, an intrinsic delay and a gate load delay for the total capacitance as a load. (See summary). Muddu teaches as the output voltage response $V_B(t)$ changes, it passes through threshold points $t=t_0$ and t_{thd} set for determining the gate response delay (slew rate). Finally, Muddu teaches that the effective capacitance is determined in the range between the step input capacitance C_{step} and the total load capacitance C_{tot} under full load conditions. It may be recalled that, under no load condition, the gate response is fast since the gate will not see the interconnect load capacitance. Under full load conditions, the gate response is slow because it needs to charge a full capacitance load. The range between C_{step} and C_{tot} is set by obtaining the intrinsic gate delay D_{NL} and the gate load delay D_{LD}. The intrinsic gate delay D_{NL} is a gate response delay with no load at the gate output, and the gate load delay D_{LD} is a gate response delay with C_{tot} as a load. (See section A. starting col.

Muddu does not explicitly teach determining a plurality of effective driving currents. Since the effective capacitance is determined in the range between the step input capacitance C_{step} and the total load capacitance C_{tot} under full load conditions and the gate response is depending on charging of capacitance load, it would have obvious to one of ordinary skill in the art to determining a plurality of effective driving currents based on characterization model and determining timing delay parameters from said effective driving currents to thereby determine timing delay including intrinsic delay and gate load delay for specific loads.

7. As to claims 10, 22, 5 and 17, Muddu teaches estimating interconnect capacitive effects including determining an effective capacitance that represents the interconnect capacitive effects at an output of a driving gate, where the effective capacitance estimation precedes by a gate load modeling. Estimating the interconnect capacitive effects includes modeling the gate using an equivalent circuit, and modeling the gate load at an output of the gate includes determining RC model parameters that represent the load at the output of the gate output. These parameters are associated with response at the gate output. Muddu teaches determining delay taking accounts for the input voltage waveform (input signal slew rate), voltage response at the gate output and RC model parameters. The effective capacitance estimation method further includes modeling a single capacitance load at the output of the gate, where the single capacitive load modeling includes determining a gate delay for a threshold time at a threshold voltage. The effective capacitance is then derived taking into account the single capacitance, a total capacitance of the gate load, an intrinsic delay and a gate load

delay for the total capacitance as a load. (See summary). Muddu teaches as the output voltage response $V_B(t)$ changes, it passes through threshold points $t=t_0$ and t_{thd} set for determining the gate response delay (slew rate). Finally, Muddu teaches that the effective capacitance is determined in the range between the step input capacitance C_{step} and the total load capacitance C_{tot} under full load conditions. It may be recalled that, under no load condition, the gate response is fast since the gate will not see the interconnect load capacitance. Under full load conditions, the gate response is slow because it needs to charge a full capacitance load. The range between C_{step} and C_{tot} is set by obtaining the intrinsic gate delay D_{NL} and the gate load delay D_{LD}. The intrinsic gate delay D_{NL} is a gate response delay with no load at the gate output, and the gate load delay D_{LD} is a gate response delay with C_{tot} as a load. (See section A. starting col. Muddu does not explicitly teach determining operation of said circuit at a new time instance based on said load capacitance of a previous time instance. Since the effective capacitance is determined in the range between the step input capacitance C_{step} and the total load capacitance C_{tot} under full load conditions and the gate response is depending on charging of capacitance load, it would have obvious to one of ordinary skill in the art to determine operation of the circuit at new time instance based on the load capacitance of a previous time instance based on operation of the circuit and response to RC network at said time instance to thereby determine timing delay including intrinsic delay and gate load delay for specific loads.

Allowable Subject Matter

8. Claim 25 is allowed.

9. Claims 2-4, 6-7, 9, 11, 12, 14, 16, 18-21 and 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (703) 305-4958. The examiner can normally be reached on M-F (6:30-4:00) 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Vuthe Siek
Primary Examiner
January 20, 2003

VUTHE SIEK
PRIMARY EXAMINER